

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
		1 and (insulat\$3 dielectric) with (recess trench hole via groove opening pore damascene))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 06:40
		(insulat\$3 electrode) with (recess trench hole via groove opening pore damascene)) with (capacitor memory)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 06:39
		IN ADJ VITRO WITH MONITOR\$3).CLM	US-PGPU B; USPAT	OR	ON	2004/11/24 12:03
		("(microadstructuremicrostructure)with(gripermanipulator)").PN.	US-PGPU B; USPAT; USOCR	OR	OFF	2004/11/24 10:53
L1	19704	(electrode with (recess trench hole via groove opening pore damascene)) with (capacitor memory)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 06:39
L2	11969	1 and ((insulat\$3 dielectric) with (recess trench hole via groove opening pore damascene))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 06:42
L3	2160	"3" and ((phase adj chang\$3 chacogenide) with (recess trench hole via groove opening pore damascene))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 06:43
L4	54	2 and ((phase adj chang\$3 chacogenide) with (recess trench hole via groove opening pore damascene))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 10:19
L5	5496572	"10"/ "319751"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 07:04
L6	0	'10/ 319750'	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 07:05
L7	119	phase adj change adj memory ti.	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 07:05
L8	11	"6511862"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 08:46

L9	1	"20040042329".PN.	US-PGPU B	OR	ON	2004/11/29 08:41
L10	1	"20030221718".PN.	US-PGPU B	OR	ON	2004/11/29 08:42
L11	1	"5395797".PN.	USPAT; USOCR	OR	ON	2004/11/29 08:42
L12	1	"5468652".PN.	USPAT; USOCR	OR	ON	2004/11/29 08:42
L13	1	"6815704"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:29
L14	1	"20030209746".PN.	US-PGPU B	OR	ON	2004/11/29 09:18
L15	1	"6605527".PN.	USPAT; USOCR	OR	ON	2004/11/29 09:19
L16	1	"6511862".PN.	USPAT; USOCR	OR	ON	2004/11/29 09:19
L17	1	"6511862".PN.	USPAT; USOCR	OR	ON	2004/11/29 09:19
L18	1	"5536947".PN.	USPAT; USOCR	OR	ON	2004/11/29 09:20
L19	1	"6511862".PN.	USPAT; USOCR	OR	ON	2004/11/29 09:22
L20	3	"10209204"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:30
L21	1	"10318704"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:31
L22	1	"10/318704"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:33
L23	1	"10319183"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:33
L24	1	"10/319183"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:34
L25	1	10/364141	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:35

L26	0	10/634141	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:35
L27	1	"10822361"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:35
L28	1	"10/822361"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:36
L29	0	10/939145	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:38
L30	17	"5538592"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:38
L31	5	"5562770"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:38
L32	1	"6294449"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:39
L33	3	"6294817"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:39
L34	1	"6686617"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:41
L35	1	"6544874"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:41
L36	1	"6773570"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:42
L37	1	10/394975	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 09:42
L38	121	2 and ((phase adj chang\$3 chalcogenide) with (recess trench hole via groove opening pore damascene))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 10:19
L39	1	"6083821".PN	USPAT; USOCR	OR	ON	2004/11/29 10:40

S1	71993	(method process\$3) with (side adj wall sidewall spacer)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/06/06 10:43
S2	10472	((method process\$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/05/27 09:43
S3	8483	((method process\$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and ((etch\$3) with (side adj wall sidewall spacer))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/05/27 09:44
S4	3612	((method process\$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch\$3 with (plasma vapor))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/05/27 08:42
S5	1636	((method process\$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch\$3 with (plasma vapor))) and (substrate with (anneal\$3 heat\$3 themal\$5 temperature))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/05/27 09:45
S6	1636	((method process\$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch\$3 with (plasma vapor))) and (substrate with (anneal\$3 heat\$3 themal\$5 temperature))) and (substrate anneal\$3 heat\$3 themal\$5 temperature gate dielectric oxide sidewall spacer side wall plasma vapor etching etch\$2 gate)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/05/27 09:45

S7	364	((((method process\$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch\$3 with (plasma vapor))) and (substrate with (anneal\$3 heat\$3 themal\$5 temperature))) and (substrate anneal\$3 heat\$3 themal\$5 temperature gate dielectric oxide sidewall spacer side wall plasma vapor etching etch\$2 gate)) and ((rotation\$2 rotat\$2 rotating spin\$4 turning turn\$3) with substrate)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/05/27 08:50
S8	99	((((method process\$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch\$3 with (plasma vapor))) and (substrate with (anneal\$3 heat\$3 themal\$5 temperature))) and (substrate anneal\$3 heat\$3 themal\$5 temperature gate dielectric oxide sidewall spacer side wall plasma vapor etching etch\$2 gate)) and ((rotation\$2 rotat\$2 rotating spin\$4 turning turn\$3) with substrate)) and (acid with etch\$3)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/05/27 08:51
S9	10135	(method process\$3) with ((side adj wall sidewall spacer) with (gate transistor))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/05/27 09:41
S10	28954	((side adj wall sidewall spacer) with (gate transistor))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/05/27 09:43
S11	22184	(((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat\$3 oxide) with gate)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/05/27 09:44

S12	13851	((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat\$3 oxide) with gate)) and ((etch\$3) with (side adj wall\$1 sidewall\$1 spacer\$1))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/05/27 09:45
S13	4977	((((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat\$3 oxide) with gate)) and ((etch\$3) with (side adj wall\$1 sidewall\$1 spacer\$1))) and (substrate with (anneal\$3 heat\$3 themal\$5 temperature)))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/05/27 09:46
S14	4977	((((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat\$3 oxide) with gate)) and ((etch\$3) with (side adj wall\$1 sidewall\$1 spacer\$1))) and (substrate with (anneal\$3 heat\$3 themal\$5 temperature))) and (substrate anneal\$3 heat\$3 themal\$5 temperature gate dielectric oxide sidewall spacer side wall plasma vapor etching etch\$2 gate insulat\$3)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/05/27 09:48
S15	2079	((((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat\$3 oxide) with gate)) and ((etch\$3) with (side adj wall\$1 sidewall\$1 spacer\$1))) and (substrate with (anneal\$3 heat\$3 themal\$5 temperature))) and (substrate anneal\$3 heat\$3 themal\$5 temperature gate dielectric oxide sidewall spacer side wall plasma vapor etching etch\$2 gate insulat\$3)) and (wet near\$5 etch\$3)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2003/05/27 09:48
S16	0	10/634139	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 11:47

S17	1	"10275978"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 11:48
S18	0	"10275978"	USPAT	OR	ON	2004/11/24 11:48
S19	0	"10/275978"	USPAT	OR	ON	2004/11/24 11:48
S20	1	"10/275978"	US-PGPU B; USPAT	OR	ON	2004/11/24 11:50
S21	2	"6180562"	US-PGPU B; USPAT	OR	ON	2004/11/24 11:54
S22	3	"6057266"	US-PGPU B; USPAT	OR	ON	2004/11/24 11:55
S23	2	"5668082"	US-PGPU B; USPAT	OR	ON	2004/11/24 11:56
S24	9	"5653054"	US-PGPU B; USPAT	OR	ON	2004/11/24 12:01
S25	958	'IN VITRO' WITH BIOLOGY\$3	US-PGPU B; USPAT	OR	ON	2004/11/24 12:02
S26	0	'IN VITRO' WITH BIOLOGY\$3.CLM.	US-PGPU B; USPAT	OR	ON	2004/11/24 12:02
S27	0	'IN VITRO' WITH MONITOR.CLM.	US-PGPU B; USPAT	OR	ON	2004/11/24 12:02
S28	0	'IN VITRO' WITH MONITOR\$3.CLM.	US-PGPU B; USPAT	OR	ON	2004/11/24 12:02
S29	0	(IN ADJ VITRO WITH MONITOR\$3).CLM.	US-PGPU B; USPAT	OR	ON	2004/11/24 12:03
S30	255	(IN ADJ VITRO WITH MONITOR\$3)	US-PGPU B; USPAT	OR	ON	2004/11/24 12:15
S31	1	"6552209"	US-PGPU B; USPAT	OR	ON	2004/11/24 12:15
S32	185	(phase adj change) with capacitor	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/29 06:37
S33	1482	(phase adj change) with memory	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 14:16
S34	1	S16 or S17	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 14:16

S35	1661	S32 or S33	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 14:16
S36	1661	S35 and (phase adj change capacitor memory)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 14:23
S37	416	"22" and ((phase adj change) with electrode)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 14:19
S38	182	S36 and ((phase adj change) with electrode)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 14:19
S39	121	S38 and ((recess trench hole via groove opening) with electrode)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 14:21
S40	131	S38 and ((recess trench hole via groove opening pore damascene) with electrode)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 14:23
S41	2081	438/259,270.ccls.	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 14:22
S42	0	S41 and S36	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 14:22
S43	592	S41 and (phase adj change capacitor memory)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 14:23
S44	246	S43 and ((recess trench hole via groove opening pore damascene) with electrode)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 14:58
S45	2	S43 and (phase adj change)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 14:59
S46	0	S41 and ((phase adj change) with (memory capaitor material layer))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 15:00
S47	10493	((phase adj change) with (memory capaitor material layer))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 15:01

S48	40	((phase adj change) with (memory capaitor material layer)) with (electrode near5 (recess trench pore damascene hole opening groove aperture))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2004/11/24 15:03
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